

**Serial No. 10/646,688**

**Listing of Claims**

1. (Currently Amended) A method for performing defect analysis, comprising:  
applying a test signal to a circuit;  
obtaining a signal generated in response to the test signal;  
comparing the response signal to reference information;  
classifying a defect in the circuit based on a result of the comparing step; and  
identifying a problem in a manufacturing process which caused the defect based on said defect classification, wherein the problem in the manufacturing process is identified by:  
comparing the defect classification to statistical information which links a plurality of predefined defect classifications to a plurality of corresponding manufacturing process problems.
2. (Original) The method of claim 1, wherein the reference information includes a signal profile of a type of defect that can occur during the manufacturing process.
3. (Original) The method of claim 2, further comprising:  
forming the signal profile from defect signals generated from previous tests of circuits that correspond to said type of defect.
4. (Original) The method of claim 3, wherein the signal profile is a statistical representation of the defect signals from said previous tests.

**Serial No. 10/646,688**

5. (Original) The method of claim 2, further comprising:  
computing a mean of signal values for a non-defective circuit; and  
forming the signal profile of said type of defect based on the computed mean value.
6. (Original) The method of claim 2, wherein said classifying step includes:  
determining that the circuit has said type of defect if the response signal falls within the  
signal profile.
7. (Original) The method of claim 1, further comprising:  
storing, in a memory, information linking a plurality of defect classifications with a  
respective plurality of manufacturing process problems, said identifying step including identifying  
said manufacturing process problem based on said linking information.
8. (Original) The method of claim 1, further comprising:  
identifying an area within said manufacturing process where the classified defect occurred.
9. (Original) The method of claim 1, further comprising:  
adjusting said process to avoid the problem during manufacture of other circuits.

**Serial No. 10/646,688**

10. (Original) The method of claim 1, wherein the reference information includes a plurality of signal profiles corresponding to different types of defects that can occur during the manufacturing process.
11. (Original) The method of claim 10, wherein the classifying step includes:  
determining that a signal profile which closely matches the response signal; and  
determining that the circuit includes the defect corresponding to the signal profile.
12. (Original) The method of claim 11, wherein the signal profile is determined to closely match the response signal when the response signal lies within the signal profile.
13. (Original) The method of claim 10, wherein the classifying step includes:  
determining that the response signal falls within two signal profiles;  
determining that one of the two profiles has a higher probability of occurrence; and  
determining that the circuit includes the defect which corresponds to the profile having the higher probability of occurrence.
14. (Original) The method of claim 13, further comprising:  
determining that the other one of the two profiles has a lower probability of occurrence based on an absence of detection of one or more other types of defects in the circuit.

**Serial No. 10/646,688**

15. (Original) The method of claim 13, further comprising:

determining that the other one of the two profiles has a lower probability of occurrence based on an absence of detection of one or more predetermined manufacturing process problems.

16. (Original) The method of claim 10, wherein the signal profiles are included in respective signal zones, said zones including ranges of signal values which respectively correspond to the different types of defects.

17. (Original) The method of claim 16, wherein the classifying step includes:

determining a signal profile range that includes the response signal; and

determining that the electrical circuit includes the defect that corresponds to the signal profile range which includes the response signal.

18. (Original) The method of claim 17, wherein the classifying step includes:

determining that the response signal lies within two signal profile ranges; and

selecting the defect that corresponds to the signal profile range having a greater probability of occurrence.

19. (Original) The method of claim 18, wherein the greater probability of occurrence is determined based on Bayes' Theorem.

**Serial No. 10/646,688**

20. (Original) The method of claim 16, further comprising:  
locating an intersection between adjacent signal profiles; and  
adjusting a position of a dividing line between signal zones corresponding to said adjacent profiles so that the error distribution of the adjacent signal profiles is at least substantially equal.
21. (Original) The method of claim 16, further comprising:  
positioning a dividing line between adjacent signal zones based on an intersection between curves included in the signal zones.
22. (Currently Amended) A method for performing defect analysis, comprising:  
detecting a pixel voltage output from a TFT array in response to a test signal;  
comparing the pixel voltage to at least one defect signal;  
classifying a defect in the array based on a result of the comparing step; and  
identifying a manufacturing process problem which caused the defect based on said defect classification, wherein the problem in the manufacturing process is identified by:  
comparing the defect classification to statistical information which links a plurality of predefined defect classifications to a plurality of corresponding manufacturing process problems.
23. (Original) The method of claim 22, wherein the defect signal corresponds to a predefined type of defect.

**Serial No. 10/646,688**

24. (Original) The method of claim 23, further comprising:  
forming the defect signal from previous test data.
25. (Original) The method of claim 23, wherein the defect signal includes a curve located within  
a signal zone corresponding to said predefined type of defect.
26. (Original) The method of claim 25, wherein the classifying step includes determining whether  
the pixel voltage falls within the curve of the defect signal.
27. (Original) The method of claim 22, further comprising:  
comparing the pixel voltage to a plurality defect signals each corresponding to a different  
type of defect, said classifying step including determining that the pixel voltage at least substantially  
matches at least one of the defect signals.
28. (Original) The method of claim 27, further comprising:  
storing information linking the different defect types to manufacturing process problems, said  
identifying step including identifying said manufacturing process problem based on said linking  
information.
29. (Original) The method of claim 22, further comprising:  
identifying an area within said manufacturing process where the classified defect occurred.

**Serial No. 10/646,688**

30. (Currently Amended) A system for performing defect analysis, comprising:
- a signal generator which applies a test signal to a circuit;
  - a detector which obtains a signal generated in response to the test signal; and
  - a processor which compares the response signal to reference information, classifies a defect in the circuit based on a result of the comparison, and identifies a problem in a manufacturing process which caused the defect based on said defect classification, wherein the processor identifies the problem in the manufacturing process by:
    - comparing the defect classification to statistical information which links a plurality of predefined defect classifications to a plurality of corresponding manufacturing process problems.
31. (Original) The system of claim 30, wherein the reference information includes a signal profile of a type of defect that can occur during the manufacturing process.
32. (Original) The system of claim 31, wherein the signal profile is generated based on previous test data.
33. (Original) The system of claim 32, wherein the signal profile is a statistical representation of the defect signals from said previous tests.
34. (Original) The system of claim 31, wherein the processor classifies the defect by determining whether the response signal falls within said signal profile.

Serial No. 10/646,688

35. (Original) The system of claim 30, further comprising:

a memory which stores information linking a plurality of defect classifications with a respective plurality of manufacturing process problems, said processor identifying the manufacturing process problem based on said linking information.

36. (Original) The system of claim 30, wherein the processor identifies an area within said manufacturing process where the classified defect occurred.

37. (Canceled)

38. (Previously Presented) The method of claim 1, further comprising:

determining in what stage of the manufacturing process the defect occurred.

39. (Currently Amended) A The method of claim 1 for performing defect analysis, comprising:

applying a test signal to a circuit;

obtaining a signal generated in response to the test signal;

comparing the response signal to reference information;

classifying a defect in the circuit based on a result of the comparing step; and



Serial No. 10/646,688

identifying a problem in a manufacturing process which caused the defect based on said defect classification, wherein the problem in the manufacturing process is automatically identified using a rules-based or knowledge-based system that associates the defect classification with one or more other defects that are likely to occur together.

40. (Previously Presented) The method of claim 1, further comprising:

determining a technique for correcting the defect classification based on the identified manufacturing process problem.

41. (Canceled)

42. (Previously Presented) The method of claim 22, further comprising:

determining in what stage of the manufacturing process the defect occurred.

43. (Currently Amended) A The method of claim 22, for performing defect analysis, comprising:

detecting a pixel voltage output from a TFT array in response to a test signal;

comparing the pixel voltage to at least one defect signal;

classifying a defect in the array based on a result of the comparing step; and

identifying a manufacturing process problem which caused the defect based on said defect classification, wherein the problem in the manufacturing process is automatically identified using a

**Serial No. 10/646,688**

rules-based or knowledge-based system that associates the defect classification with one or more other defects that are likely to occur together.

44. (Previously Presented) The method of claim 22, further comprising:  
determining a technique for correcting the defect classification based on the identified manufacturing process problem.
45. (Canceled)
46. (Previously Presented) The system of claim 30, wherein the processor determines in what stage of the manufacturing process the defect occurred.
47. (Currently Amended) A The system of claim 30, for performing defect analysis, comprising:  
a signal generator which applies a test signal to a circuit;  
a detector which obtains a signal generated in response to the test signal; and  
a processor which compares the response signal to reference information, classifies a defect in the circuit based on a result of the comparison, and identifies a problem in a manufacturing process which caused the defect based on said defect classification, wherein the processor determines the problem in the manufacturing process by referencing a rules-based or knowledge-based system that automatically associates the defect classification with one or more other defects that are likely to occur together.

**Serial No. 10/646,688**

48. (Previously Presented) The system of claim 30, wherein the processor determines a technique for correcting the defect classification based on the identified manufacturing process problem.